said T-RAM cells.

REMARKS

Applicants elected Group II (Claims 12-17) without traverse in response to Examiner's restriction requirement. Claims 1-11 and 18-28 were withdrawn from consideration by examiner as being drawn to a non-elected invention.

The informal drawings were objected to by the draftsperson. Formal drawings are enclosed herewith.

Claim 17 was rejected under 35 USC §112, second paragraph. Claim 17 has been amended to overcome this rejection. Claim 17 is now believed to be in compliance with 35 USC §112, and this rejection should be withdrawn.

Claims 12-17 were rejected under 35 USC §103(a) for allegedly being unpatentable over U.S. Patent No. 6,448,586 ("Nemati"). Claims 12, 13, 15, 16, and 17 have been amended and Claims 29-30 have been added to distinguish over this reference.

Claim 12 recites "a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and fabricated over a substrate, each of said plurality of T-RAM cells including a first and a second device, said first device being buried underneath said second device, wherein said second device covers the entire top surface of said first device, and further wherein the top surface of said second device forms a planar top surface of each said T-RAM cell".

Nemati does not disclose, teach, or suggest a first device being buried underneath a second device wherein the second device covers the entire top surface of the first device as

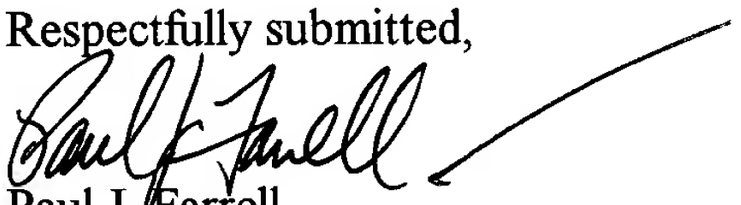
is recited in Claim 12. Nemati also does not disclose, teach, or suggest a T-RAM cell having a planar top surface as is recited in Claim 12. To the contrary, Nemati is directed to a first device being located at least partially adjacent to a second device. Specifically, Nemati is directed to a combination of a horizontal gate device (Fig. 1, #12) and a vertical thyristor device (Fig. 1, #10) being located at least partially adjacent to one another and thereby forming a non-planar surface. For at least these reasons, it is submitted that Claim 12 would not have been obvious to one of ordinary skill in the art and is therefore is

patentable over Nemati. Moreover, it is also submitted that claims 14-17, by virtue of their dependency upon claim 12, are also patentable over Nemati.

Referring now to Claim 13, Claim 13 recites a "...said first device is a buried vertical thyristor and said second device is a horizontal transfer gate". Nemati does not disclose, teach, or suggest said first device being a buried vertical thyristor and said second device being a horizontal transfer gate. For at least these reasons and the reasons described above for Claim 12, Applicants submit that the invention recited in claim 13 would not have been obvious to one of ordinary skill in the art and thus is patentable over Nemati.

Applicants submit that pending Claims 12-17 and 29-30 are now believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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Marked-Up Version of the Claims

12. (Amended) [A] An array of planar T-RAM [array] cells comprising:

a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and fabricated over a substrate, each of said [wherein each of the] plurality of T-RAM cells [includes] including [a thyristor region beneath at least a portion of a transfer gate region] a first and a second device, said first device being buried underneath said second device, wherein said second device covers the entire top surface of said first device, and further wherein the top surface of said second device forms a planar top surface of each said T-RAM cell.

13. (Amended) The array according to Claim 12, wherein said first device is a [the thyristor region includes a] buried vertical thyristor and said second device is a horizontal [the transfer gate region includes a horizontally stacked pseudo-TFT] transfer gate.

15. (Amended) The array according to Claim 12, wherein [the plurality of T-RAM cells are fabricated on a] said substrate is a semiconductor SOI or bulk wafer.

16. (Amended) The array according to Claim [12] 13, wherein a base of [the] said thyristor [region] is surrounded by a surrounded gate.

17. (Amended) The array according to Claim 12, wherein [each of the plurality of T-RAM cells includes structure for the traversal of at least two wordlines there through] said planar top surface of each T-RAM cell provides for simplified fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-RAM cells, said wirings for interconnecting said T-RAM cells.